UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,237	01/14/2004	Jimmie Earl DeWitt JR.	AUS920030550US1	3251

35525 7590 10/05/2006

IBM CORP (YA)
C/O YEE & ASSOCIATES PC
P.O. BOX 802333
DALLAS, TX 75380

EXAMINER	
LAI, VINCENT	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,237	DEWITT ET AL.	
	Examiner	Art Unit	
	Vincent Lai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within,the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
9/28/2006

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/25/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 1/14/2004 was considered by the examiner.

Response to Amendment

2. Acknowledgement is made of the amendments to the specification, title, and claims.

3. As stated in the Interview Summary, an erroneous objection to the drawings was made and has been withdrawn.

4. Objections to title and specification are withdrawn after considering amendments.

5. 35 USC 112 rejections and 35 USC 101 rejections are withdrawn after considering amendments.

Response to Arguments

6. Applicant's arguments filed 13 July 2006 have been fully considered but they are not persuasive.

After further review of the amended claims and the remarks submitted, Examiner is not persuaded by arguments submitted. It would appear that new limitations to the claims would be obvious to one having ordinary skill in the art at the time the invention was made. Using the reasoning present on page 12 of the remarks, Examiner intended to show how one having ordinary skill in the art would be led to modify Holmberg to cover the limitations of claims in application. These arguments are presented below.

Claim Objections

Claims 6, 9, 13, and 20 are objected to because of the following informalities:

The claims state "the plurality of branch statistics are," which is grammatically incorrect and suggested to be changed to "the plurality of branch statistics is."

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holmberg (U.S. Patent # 6,233,679 B1).

As per **claim 1**, Holmberg teaches a method of performing branch prediction (See column 3, lines 35-37: Branch prediction is the main purpose of the Holmberg invention) in a computer program, comprising the steps of:

identifying a plurality of branch instructions for application code being complied (See column 3, lines 50-52: Processor identifies type of instruction and thus will know which are branch instructions);

associating a plurality of hardware counters with the plurality of branch instructions (See column 4, lines 56-63: Multiple counters are used—each for counting various actions);

using the plurality hardware counter to autonomically count branch instructions that are executed in parallel to generate a plurality of branch statistics (See column 4, lines 64-65: Counters are used from providing statistics);

predicting branches to be taken using the plurality of branch statistics (See column 4, lines 64-65: Counter statistics are used to set branch prediction bits) to form branch predictions; and

prefetching the plurality of branch instructions using the plurality of branch predictions (See column 4, lines 1-3).

Holmberg does not teach counting all of the plurality of branch instructions that are executed in parallel.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Holmberg such that counting all of the plurality of branch instructions that are executed in parallel would be done. Holmberg teaches that statistics should be collected for all conditional branches (See column 2, lines 60-64) and that braches are to be run in parallel (See column 2, lines 50-53). This would necessitate the need/desire to count all branch instructions in parallel. Holmberg goes on to teach the use of a plurality of hardware counters for collecting statistics for the plurality of branch instructions (See column 2, lines 66-67), thus suggesting that it there is a desire to count all of the plurality of branch instructions that are executed in parallel.

As per **claim 2**, Holmberg teaches wherein the one or more branch instructions are associated with plurality of branch statistics (See column 4, line 54-column 5, line 2: Three types of counts are counter), and wherein the plurality of branch statistics are stored in a plurality of branch statistic fields (See figure 2, element 121 and column 4, lines 46-52: The branch statistics are saved in special registers).

As per **claim 3**, Holmberg teaches wherein the plurality of branch statistic fields store a plurality of data on an associated branch instruction (See column 4, lines 56-63: Multiple counters are used—each for counting various actions), wherein a first datum of the plurality of data is accessed for branch prediction when the program is in a first mode (See column 5, lines 35-43: First mode is branch predicted to be taken), and wherein a second datum of the plurality of data is accessed for branch prediction when

the program is in a second mode (See column 5, lines 35-44: Second mode is branch predicted to be not taken).

As per **claim 4**, Holmberg teaches wherein the plurality of branch statistic fields include a branch count per instruction field that represents the number of times a branch is taken for that instruction (See column 4, lines 64-67: Statistics count number of times a branch is taken).

As per **claim 5**, Holmberg teaches wherein upon occurrence of a predetermined event, the computer program switches branch prediction operating modes on a conditional branch instruction (See figure 3, and column 5, lines 35-44: A new prediction is made if a counter threshold is passed).

As per **claim 6**, Holmberg teaches wherein the plurality of branch statistics are stored in a performance instrumentation shadow cache (See column 4, lines 47-55: The shadow cache is known as the Measured Address Register (MAR)).

As per **claim 7**, Holmberg teaches wherein branches per instruction are counted during execution of the computer program (See column 4, line 64-column 5, line 2: The total number of branches is one of the counts tracked).

As per **claim 8**, Holmberg teaches a branch prediction apparatus, comprising:

a complier that identifies a plurality of branch instructions for application code being complied (See column 3, lines 50-52: Processor identifies type of instruction and thus will know which are branch instructions);

a plurality of hardware counters associated with the plurality of branch instructions of the application code (See column 4, lines 56-63: Multiple counters are used—each for counting various actions);

a plurality of branch statistic fields for storing a plurality of branch statistics associated with the plurality of branch instructions (See column 4, line 54-column 5, line 2: Three types of counts are counter);

wherein when a branch instruction in the plurality of branch instructions is executed in the application code, a hardware counter of the plurality of hardware counters autonomically updates in parallel branch statistics in the plurality of branch statistic fields (See figure 3, and column 5, lines 35-44: The branch prediction mechanism is set up to track statistics and changes predictions automatically);

a processor that predicts branches to be taken using the plurality of branch statistics to form branch predictions (See column 4, lines 1-3); and

the processor prefetches the plurality of branch instructions using the branch predictions (See column 4, lines 1-3).

Holmberg does not teach counting all of the plurality of branch instructions that are executed in parallel.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Holmberg such that counting all of the plurality

of branch instructions that are executed in parallel would be done. Holmberg teaches that statistics should be collected for all conditional branches (See column 2, lines 60-64) and that braches are to be run in parallel (See column 2, lines 50-53). This would necessitate the need/desire to count all branch instructions in parallel. Holmberg goes on to teach the use of a plurality of hardware counters for collecting statistics for the plurality of branch instructions (See column 2, lines 66-67), thus suggesting that it there is a desire to count all of the plurality of branch instructions that are executed in parallel.

As per **claim 9**, Holmberg teaches wherein the plurality of branch statistics are used to make branch predictions in the application code (See column 4, lines 64-65: Counter statistics are used to set branch prediction bits).

As per **claim 10**, Holmberg teaches further comprising a plurality of operating modes of the application code, wherein for a first branch instruction, an associated branch statistics field stores first branch statistics for a first mode of the plurality of operating modes (See column 5, lines 35-43: First mode is branch predicted to be taken), and second branch statistics for a second mode of the plurality of operating modes (See column 5, lines 35-44: Second mode is branch predicted to be not taken).

As per **claim 11**, Holmberg teaches wherein the plurality of branch statistic fields include a branch count per instruction field that represents the number of times a branch

is taken for that branch instruction (See column 4, lines 64-67: Statistics count number of times a branch is taken).

As per **claim 12**, Holmberg teaches wherein upon occurrence of a predetermined event, the program switches branch prediction operating modes on a conditional branch instruction (See figure 3, and column 5, lines 35-44: A new prediction is made if a counter threshold is passed).

As per **claim 13**, Holmberg teaches wherein the plurality of branch statistics are stored in a performance instrumentation shadow cache (See column 4, lines 47-55: The shadow cache is known as the Measured Address Register (MAR)).

As per **claim 14**, Holmberg teaches wherein branches per instruction are counted during execution of the program (See column 4, line 64-column 5, line 2: The total number of branches is one of the counts tracked).

As per **claim 15**, Holmberg teaches a computer program product in a recordable-type computer readable medium, comprising:

instructions for identifying a plurality of branch instructions for application code being complied (See column 3, lines 50-52: Processor identifies type of instruction and thus will know which are branch instructions);

instructions for associating a plurality of hardware counters with the plurality of branch instructions (See column 4, lines 56-63: Multiple counters are used—each for counting various actions);

instructions for autonomically counting all of the plurality of branch instructions that are executed in parallel using the plurality of hardware counters to thereby generate a plurality of branch statistics (See column 4, lines 64-65: Counters are used from providing statistics);

instructions for predicting branches to be taken using the plurality of branch statistics to form branch predictions (See column 4, lines 64-65: Counter statistics are used to set branch prediction bits); and

instructions for executing the application code using the branch predictions (See column 4, lines 1-3).

Holmberg does not teach counting all of the plurality of branch instructions that are executed in parallel.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Holmberg such that counting all of the plurality of branch instructions that are executed in parallel would be done. Holmberg teaches that statistics should be collected for all conditional branches (See column 2, lines 60-64) and that braches are to be run in parallel (See column 2, lines 50-53). This would necessitate the need/desire to count all branch instructions in parallel. Holmberg goes on to teach the use of a plurality of hardware counters for collecting statistics for the

plurality of branch instructions (See column 2, lines 66-67), thus suggesting that it there is a desire to count all of the plurality of branch instructions that are executed in parallel.

As per **claim 16**, Holmberg teaches wherein the plurality of branch instructions are associated with the plurality of branch statistics (See column 4, line 54-column 5, line 2: Three types of counts are counter), and wherein the plurality of branch statistics are stored in the plurality of branch statistic fields (See figure 2, element 121 and column 4, lines 46-52: The branch statistics are saved in special registers).

As per **claim 17**, Holmberg teaches wherein the plurality of branch statistic fields store a plurality of data on an associated branch instruction (See column 4, lines 56-63: Multiple counters are used—each for counting various actions), wherein a first datum of the plurality of data is accessed for branch prediction when the program is in a first mode (See column 5, lines 35-43: First mode is branch predicted to be taken), and wherein a second datum of the plurality of data is accessed for branch prediction when the program is in a second mode (See column 5, lines 35-44: Second mode is branch predicted to be not taken).

As per **claim 18**, Holmberg teaches wherein the plurality of branch statistic fields include a branch count per instruction field that represents the number of times a branch is taken for that branch instruction (See column 4, lines 64-67: Statistics count number of times a branch is taken).

As per **claim 19**, Holmberg teaches wherein upon occurrence of a predetermined event, the computer program switches branch prediction operating modes on a conditional branch instruction (See figure 3, and column 5, lines 35-44: A new prediction is made if a counter threshold is passed).

As per **claim 20**, Holmberg teaches wherein the plurality of branch statistics are stored in a performance instrumentation shadow cache (See column 4, lines 47-55: The shadow cache is known as the Measured Address Register (MAR)).

As per **claim 21**, Holmberg teaches wherein branches per instruction are counted during execution of the computer program (See column 4, line 64-column 5, line 2: The total number of branches is one of the counts tracked).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Lai
Examiner
Art Unit 2181

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

vl
September 27, 2006